

## METAL GATE ENGINEERING FOR SURFACE P-CHANNEL DEVICES

### Abstract of the Disclosure

A semiconductor device, such as a CMOS device, having gates with a high work function in PMOS regions and low work functions in NMOS regions and a method of producing the same. Using nitrogen implantation or plasma annealing, a low work function W (or  $\text{CoSi}_x$ )/ $\text{TaSi}_x\text{N}_y$ /GOx/Si gate stack is formed in the NMOS regions while a high work function W (or  $\text{CoSi}_x$ )/ $\text{Ta}_5\text{Si}_3$ /GOx/Si gate stack is formed in the PMOS regions. The improved process also eliminates the need for a nitrided GOx which is known to degrade  $g_m$  (transconductance) performance. The materials of the semiconductor devices exhibit improved adhesion characteristics to adjacent materials and low internal stress.

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